

REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-17 are presently active. No claims are amended, cancelled or added.

In the outstanding Office Action, Claims 1-17 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,563,603 to Yamazaki. Applicants respectfully traverse that rejection.

Initially, Applicants and Applicants' representative gratefully acknowledge the courtesy of a personal interview with Examiner Singh and Primary Examiner Wallerson on March 8, 2005. During the interview, the claimed invention and differences between the claimed invention and the reference cited in the outstanding Office Action were discussed. The Examiners indicated the cited references do not appear to teach or suggest the claimed inventions and they will reconsider allowability of the claims when a response is filed. Comments discussed during the interview are reiterated below.

Claim 1 is directed to an image processing apparatus that includes, *inter alia*, an entirety controlling unit and a memory unit. The entirety controlling unit is connected to at least two units out of an image reading unit, an image memory control unit, an image processing unit, and an image writing unit. The memory unit previously stores a processing information on a content of the image processing with respect to image data. The entirety controlling unit reads a part of the processing information stored in the memory unit and stores the read information in a storage unit provided in the image processing unit. The image processing unit subjects the image data to the image processing based on the processing information stored in the storage unit. Independent Claims 5, 9 and 13 include similar features.

In a non-limiting example, Applicants' Figure 2 shows an image processing apparatus that includes a process controller 211 (e.g., entirety controlling unit) and RAM 212 and ROM 213 (e.g., memory unit). The ROM 213 stores a processing information, for example procedures and parameters for processing and an image processor (e.g., a processing information on a content of the image processing with respect to the image data). The image processing apparatus of this example also includes an image processor 204 (e.g., image processing unit) that includes a program RAM 505 and a processor array 504, as shown in Applicants' Figure 5. The processor array 504 performs various processing with respect to the image data stored in the group of bus switches/local memories 502 based on the procedures and parameters for the processing in the processor stored in program RAM 505. Further, in this example the processor controller 211 (e.g., entirety controlling unit) loads the contents of the program RAM 505 from the ROM 213. In other words, the entirety controlling unit reads processing information stored in the ROM 213 (e.g., memory unit) and stores the read information in program RAM 505 in the image processor (e.g., a storage unit provided in the image processing unit).

As discussed during the interview, Yamazaki does not teach or suggest an image processing apparatus that includes an entirety controlling unit that reads a part of processing information stored in a memory unit and stores the read information in a storage unit provided in an image processing unit. Further, as discussed during the interview, Yamazaki also does not teach or suggest a memory unit that stores processing information on a content of the image processing and does not teach or suggest that an image processing unit subjects image data to image processing based on the processing information stored in the storage unit. Yamazaki in Figure 1 shows a scanner 100 that includes a CPU 138 (e.g., entirety controlling unit) connected to a memory 132 (e.g., memory unit). However, as discussed during the interview, Yamazaki does not disclose that the memory unit 132 stores any

processing information on a content of the image processing. Thus, it is respectfully submitted that Yamazaki does not teach or suggest "a memory unit which previously stores a processing information on a content of the image processing with respect to the image data," as recited in independent Claim 1 and as similarly recited in independent Claims 5, 9 and 13.

Further, Yamazaki indicates that an image processing unit 135 can perform a gamma correction. However, Yamazaki in Figure 6 does not show that image processing unit 135 includes any storage. Further, Yamazaki does not indicate that the CPU reads any processing information stored in memory 132 or stores the read information in a storage unit in image processing unit 135. Hence, Applicants respectfully submit that Yamazaki does not teach or suggest that "said entirety controlling unit reads a part of the processing information stored in said memory unit and stores the read information in a storage unit provided in said image processing unit," as recited in independent Claim 1 and as similarly recited in independent Claims 5, 9 and 13.


In addition, as discussed during the interview, Yamazaki only indicates that image processing unit 135 performs a gamma correction. Hence, Applicants respectfully submit that Yamazaki does not teach or suggest that "said image processing unit subjects the image data to the image processing based on the processing information stored in said storage unit," as recited in independent Claim 1 and as similarly recited in independent Claims 5, 9 and 13.

Accordingly, Applicants respectfully submit that independent Claims 1, 5, 9 and 13 and the claims dependent therefrom are allowable.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.



Customer Number  
22850

---

Gregory J. Maier  
Registration No. 25,599  
Surinder Sachar  
Registration No. 34,423

GJM:SS:ZSS:dnf